IN THE CLAIMS:

Claims 1 through 6, 8 through 14 and 16 through 19 are currently pending in this application. Claims 7, 15 and 20 have been cancelled without prejudice or disclaimer. Also, please amend Claims 1 through 6, 8 through 14 and 16 through 19, as follows:

1. (Currently Amended) A semiconductor device, comprising:

a non-volatile memory cell array including a plurality of word lines, a plurality of bit lines intersected with the [[a]] plurality of word lines, and a plurality of non-volatile memory cells each having a phase change resistor arranged at respective positions where the [[a]] plurality of word lines are intersected with the [[a]] plurality of bit lines;

a write buffer for supplying a write signal corresponding to write data, the write buffer being operatively connected to the non-volatile memory cell array;

an input buffer for supplying the write data to the write buffer; and

a write data register connected to the input buffer and holding the write data.

2. (Currently Amended) The [[A]] semiconductor device according to claim 1, further comprising:

an address register for holding an address ~~input from external~~; and

a comparator for comparing an address held in the address register with an input address;

wherein the semiconductor device outputs the write data held in the write data register [[if]] when the comparator indicates that the address held in the address register agrees with the input address.

3. (Currently Amended) The [[A]] semiconductor device according to claim 2, wherein the comparator makes a comparison at a subsequent read access after a write is done to the non-volatile memory cell array.

4. (Currently Amended) The [[A]] semiconductor device according to claim 2, wherein when [[if]] the comparator indicates that the address held in the address register agrees with the input address, the semiconductor device performs no read operation from the non-volatile memory cell array.

5. (Currently Amended) The [[A]] semiconductor device according to claim 4, further comprising:

a sense amplifier block which supplies a read voltage to a selected bit line of the [[a]] plurality of bit lines in the read operation;

wherein the sense amplifier block does not supply the read voltage when [[if]] the comparator indicates that the address held in the address register agrees with the input address.

6. (Currently Amended) The [[A]] semiconductor device according to claim 2 [[1]], further comprising an address transition detector which detects an address transition of an internal address by the input address.

7. (Cancelled)

8. (Currently Amended) A semiconductor device, comprising:

a memory cell array including a plurality of word lines, a plurality of bit lines which are intersected with the [[a]] plurality of word lines, and a plurality of memory cells each having a phase change resistor which are arranged at respective positions where the [[a]] plurality of word lines are intersected with the [[a]] plurality of bit lines;

a write buffer for supplying a write signal corresponding to write data, the write buffer being operatively connected to the memory cell array;

an input buffer for supplying the write data to the write buffer;

a write data register connected to the input buffer and holding the write data; and

a flag register for holding a flag,

wherein the flag indicates whether the write data held in the write data register is valid.

9. (Currently Amended) The [[A]] semiconductor device according to claim 8, wherein the flag register is set by a write operation.

10. (Currently Amended) The [[A]] semiconductor device according to claim 9, wherein the flag register is reset when the semiconductor device is powered on.

11. (Currently Amended) The [[A]] semiconductor device according to claim 9, wherein the flag register is reset when a predetermined ~~desirable~~ period of time has lapsed after the write operation.

12. (Currently Amended) The [[A]] semiconductor device according to claim 8, further comprising:

an address register for holding an address ~~input from external~~; and

a comparator for comparing an address held in the address register with the next input address;

wherein the comparator performs the comparing operation when [[if]] the flag indicates the write data is valid and does not perform the comparing operation when [[if]] the flag indicates the write data is invalid.

13. (Currently Amended) The [[A]] semiconductor device according to claim 12 [[8]], further comprising an address transition detector which detects an address transition of an internal address by the next input address.

14. (Currently Amended) The [[A]] semiconductor device according to claim 8, wherein each of the [[a]] plurality of memory cells is a non-volatile memory cell.

15. (Cancelled)

16. (Currently Amended) A semiconductor device, comprising:

a non-volatile memory cell array including a plurality of word lines, a plurality of bit lines intersected with the [[a]] plurality of word lines, and a plurality of non-volatile memory cells each having a phase change resistor arranged at respective positions where the [[a]] plurality of word lines are intersected with the [[a]] plurality of bit lines; and

a write data register for holding write data which is written into the [[a]] plurality of non-volatile memory cells;

wherein when a [[if]] write access is followed by a read access, a first address for the write access is compared with a second address for the read access and the

write data held in the write data register is read out when [[if]] the first address agrees with the second address.

17. (Currently Amended) The [[A]] semiconductor device according to claim 16, wherein the comparing operation is performed when [[if]] the write data is valid and not performed when [[if]] the write data is invalid.

18. (Currently Amended) The [[A]] semiconductor device according to claim 17, further comprising a flag which indicates whether the write data is valid or invalid;

wherein the flag indicates the write data is valid when the write access occurs and the write data [[date]] is invalid after a predetermined ~~predeterminant~~ period of time has lapsed.

19. (Currently Amended) The [[A]] semiconductor device according to claim 16, wherein a read voltage is supplied to a selected bit line of the [[a]] plurality of bit lines when data is read out from the non-volatile memory cell array whereas the read voltage is not supplied when the write data held in the write data register is read out.

20. (Cancelled)